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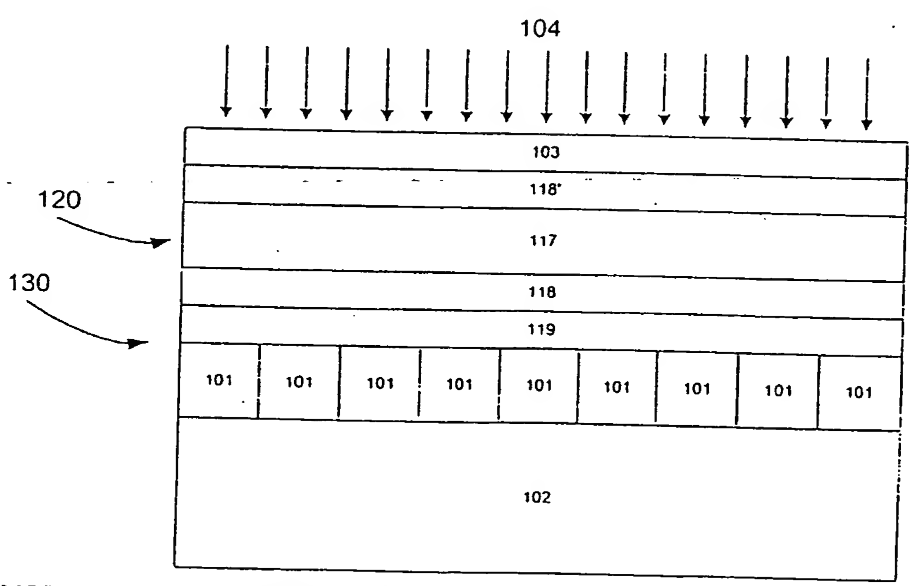
(54) Title: CMOS IMAGER FRAME CAPTURE



(57) Abstract: A CMOS imager capable of operating in a frame capture mode. The imager has an array of active pixel sensors (APS) which sense and store incident light levels at discrete points in the array and a shutter for determining the period of time that light is incident on the array. The shutter, such as a controlled liquid crystal, may be positioned on the array surface or some distance from it, allowing incident light to pass through the shutter and impinge on the array, or the shutter may be positioned at an oblique angle to the array to reflect incident light onto the array. When the APS's in the array are 4T or 5T APS's with a sensor node and a storage node, the two nodes may be connected through two or more series connected transistors or a long transistor to prevent sub-threshold currents. Also, the storage node may be connected to the gate of a feedback transistor to raise the voltage on the storage node as the voltage on the storage node degrades.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

CMOS IMAGER FRAME CAPTURE

Field of the Invention

The invention relates generally to image sensors, and more particularly to frame capture in CMOS imagers.

Background of the Invention

A CMOS imager consists of an array of active pixel sensors (APS). Each pixel includes a photosensitive semiconducting device coupled with active semiconducting elements arranged as a storage circuit and output access circuit. A common APS pixel is a 3T (three transistor) pixel. The 3T pixel is structured in the following manner:

- a reset transistor is coupled to a photodiode
- a second transistor is configured as a source follower amplifier. Its gate is connected to a common node between the reset transistor and the photodiode.
- a third transistor serves as an access transistor to allow a signal level to be transferred to a data line.

A typical active-pixel area-array image sensor is disclosed in Hurwitz et al., "An 800K-Pixel Color CMOS Sensor For Consumer Still Cameras", SPIE Vol. 3019, April 1997, pp 115-124 which is incorporated herein by reference.

A signal level representative of the intensity of light impinging on the pixel can be acquired as a proportion of the charge collected or discharged during a period of exposure. This exposure period is also know as the integration time and begins with the reset (i.e. drainage or replenishment) of all charges in the pixel and ends when the amount of charge remaining in the pixel is sampled in some manner.

Sensors can capture images using a number of techniques. Currently, the most common technique is popularly known as rolling shutter capture where one row of pixels is integrated at a time. Each row is reset in sequence and then sampled and read out, again in sequence. Rolling shutter techniques are often adequate for video applications. However, they are not always suitable for capturing still images. If the

subject of the photograph is moving during the integration period, the rolling shutter technique results in a blurred image. As the subject moves, it is in a different position when each row is integrated.

A solution to this problem is known as the frame capture method. In frame capture, each row begins integration at the same time and then is read out sequentially. This means that each pixel must sample the amount of charge present at the end of the integration period and hold that charge until that row is read out. Therefore, each pixel must retain a fixed amount of charge for an extended period of time. Traditional CMOS 3T pixels do not allow for the retention of charge for long periods of time particularly when exposed to light. Various solutions have been proposed, including CMOS 4T and 5T pixel configurations. These solutions store the charge in the pixel while isolating a storage node from the photodiode. As array sizes increase into the mega-pixel range, the amount of time required to read out the entire array is also growing. This obviously strains the limit of the charge retention capabilities of the pixels; charge leakage is still a problem, especially in the case where light is impinging on the storage node which accelerates the leakage.

Therefore, there is a need for a CMOS imager system that permits frame capture by a large array of incident light-to-charge transducer pixels while at the same time exhibits negligible charge degradation during sequential access of those pixels.

Summary of the Invention

The invention is directed to a CMOS imager having an array of active pixel sensors (APS) wherein charge level degradation is minimized during sequential access to the APS's.

In accordance with one aspect of the invention, a shutter is used to control the incident light that impinges on the array. The shutter may be a voltage or a frequency controlled liquid crystal shutter. The liquid crystal shutter may include one or more liquid crystal layers with electrodes on both sides of the layers to receive the controlling signal.

The liquid crystal shutter may be positioned substantially parallel to the APS array such that the incident light impinging upon the active pixel sensors passes through the liquid crystal shutter. The shutter may be integrated with the array or it may be fixed at some finite distance from the array surface.

In another embodiment, the liquid crystal shutter may be positioned at an oblique angle to the APS array to deflect incident light onto the array for a controlled period of time.

In accordance with another aspect of the present invention, the CMOS imager has an array of active pixel sensors (APS) which include a photodiode sensor node for integrating the incident light during a predetermined period of time, a storage node for storing charge level from the photodiode sensor node and two or more series connected transistors connected between the sensor node and the storage node to transfer the charge from the sensor node to the storage node, and to isolate the storage node from the sensing node after the transfer has been made.

In accordance with a further aspect of the present invention, the CMOS imager has an array of active pixel sensors (APS) which include a photodiode sensor node for integrating the incident light during a predetermined period of time, a storage node for storing charge level from the photodiode sensor node and a long transistor connected between the sensor node and the storage node to transfer the charge from the sensor node to the storage node, and to isolate the storage node from the sensing node after the transfer after the transfer has been made.

With regard to another aspect of this invention, the CMOS imager has an array of active pixel sensors (APS) which include a photodiode sensor node for integrating the incident light during a predetermined period of time and a storage node for storing charge level from the photodiode sensor node. The APS's further include a feedback element coupled to the storage node for increasing the voltage on the node as the charge level on the storage node degrades. The feedback element may be a transistor connected to a current source with its gate coupled to the storage node.

With respect to a specific aspect of the present invention, the APS's may be 4T or 5T APS's.

In accordance with another aspect of the present invention, a method for controlling a CMOS imager having an array of active pixel sensors (APS) for individually sensing and storing incident light levels comprises the steps of resetting the APS's substantially simultaneously, allowing incident light to impinge on the APS's for a predetermined integration period, storing the charge level of the incident light and reading out charge levels of the APS's sequentially. More specifically, the step of allowing incident light to impinge on the APS's may include the steps of opening a shutter to allow incident light to impinge on the APS array and then closing the shutter after the predetermined integration period to stop incident light from impinging on the APS array. Alternately, the step of allowing incident light to impinge on the APS's may include the steps of causing incident light to be deflected so as to impinge on the APS array; and stopping the incident light from impinging on the APS array after the predetermined integration period.

Other aspects and advantages of the invention, as well as the structure and operation of various embodiments of the invention, will become apparent to those ordinarily skilled in the art upon review of the following description of the invention in conjunction with the accompanying drawings.

Brief Description of the Drawings

The invention will be described with reference to the accompanying drawings, wherein:

Figure 1 illustrates in cross-section a prior art CMOS imager;

Figure 2 is an example of a typical CMOS 4T APS;

Figure 3 illustrates the timing information for an imager having APS's of the type shown in figure 2;

Figure 4 schematically illustrates in cross-section one embodiment of a CMOS imager with a liquid crystal shutter;

Figure 5 illustrates the timing information for a figure 4 imager;

Figure 6 schematically illustrates in cross-section a second embodiment of a CMOS imager with a liquid crystal shutter;

Figure 7 schematically illustrates in cross-section a third embodiment of a CMOS imager with a liquid crystal shutter;

Figure 8 schematically illustrates in cross-section a fourth embodiment of a CMOS imager with a liquid crystal reflector;

Figure 9 illustrates one embodiment of a CMOS APS in accordance with the present invention;

Figure 10 illustrates a second embodiment of a CMOS APS in accordance with the present invention; and

Figure 11 illustrates a third embodiment of a CMOS APS in accordance with the present invention.

Detailed Description of the Invention

Figure 1 schematically illustrates in cross-section a prior art CMOS imager 100 including APS's 101 fabricated on a silicon substrate 102. Incident light 104 passes through a transparent passivation layer 103 into the APS array 100.

A schematic of a typical CMOS 4T APS is illustrated in figure 2. Similar nMOS and pMOS APS's are described in US Patent 6,069,376 which issued on May 30, 2000 to Merrill and which is incorporated herein by reference. Incident light 104 falling on a photodiode 106 causes a discharging of a sensor node 105 between photodiode 106 and reset transistor 107. The sensornode 105 is precharged by the reset transistor 107.

The charge level is stored on a sample node 109. Access from the sample node 109 to the sensor node 105 is controlled by a sampling or storage transistor 108. The sampling node 109 is coupled to the gate of an output pull-up transistor 110. The source of transistor 110 is coupled to an output access transistor 111. The reset, sampling and output access transistors 107, 108 and 111 are controlled by reset 112, storage 113 and pixel access 114 signals, respectively. When the CMOS imager 100 is operated in the frame capture mode, common reset 112 and storage 113 signals are applied to all of the pixels in the array 100 and then a pixel access signal 114 is applied to each pixel in the array 100 sequentially to read off the specific values of the stored charge levels for the pixels.

Figure 3 shows the timing information associated with the CMOS imager 100 when operated in the frame capture mode. The integration time 115 for all of the APS's is the period of time from the end of the reset signal 112 to the beginning of the storage signal 113. The integration period 115 occurs simultaneously for all pixels.

However, each pixel has its own individual storage time116 which starts at the beginning of the storage signal and ends at the beginning of the access signal 114 for that particular pixel. As an example, storage time 116 is shown for the nth pixel of N total pixels. This is the period during which the pixel waits to be read. When the number of pixels, N, is very large, the charge degradation at the sample node 109 can become significant. The continued dissipation of charge at the sensor node 105 due to incident light after sampling causes a voltage differential across the sampling transistor 108. This, in turn leads to sub-threshold leakage that destroys the charge information at the sample node 109 over a long duration.

In a CMOS 3T APS where the charge remains on the sensing node until it is accessed, the charge has an even greater tendency to discharge through sub-threshold leakage when light continues to impinge on the photosensitive diode.

In order to alleviate this problem, a shutter mechanism may be provided such that after the entire array has been reset simultaneously, it is exposed to impinging light for an integration period after which the shutter is closed. Read out can then take place at a relatively slow rate by accessing the pixels individually by rows and columns, the rate being limited only by the dark current error in the pixels. Mechanical shutters may be possible, but not practicable, since they would add to the cost and complexity of the camera, and also contribute to camera shake. Further, the physical operation of a mechanical shutter can introduce a relative delay across the frame in high speed applications.

Figure 4 schematically illustrates a cross-section of the preferred embodiment of a CMOS imager 130 in accordance with the present invention. In addition to the APS's 101 fabricated on a silicon substrate 102 which are covered by a transparent passivation layer 103 as shown in figure 1, a shutter 120 comprising a liquid crystal layer 117 is sandwiched by 2 electrode layers 118 and 118' between the passivation layer 103 and the APS's 101. In addition, a layer of insulation 119 is required to separate the lower electrode 118 and the APS array 101. The liquid crystal shutter120, through its light transmitting properties that are electro-sensitive, may be voltage or frequency controlled to allow light to pass only during the APS integration period. In this way, degradation of sensor charge will be prevented that in turn leads to a

reduction of sub-threshold leakage. A frequency controlled liquid crystal micro-shutter system is described in US Patent 4,386,836 which issued on June 7, 1983 to Oaki et al and which is incorporated herein by reference.

The timing information associated with the CMOS imager 130 with the crystal shutter 120 is illustrated in figure 5. In addition to the reset 112, storage 113 and pixel access 114 signals which are identical in function to the corresponding signals described with respect to figure 3, a control signal 127 is generated to operate the shutter 120. Signal 127, applied to the electrode layers 118, 118', controls the transmissivity of the crystal shutter 120. The timing of signal 127 is such that it starts after the end of reset signal 112 causing the liquid crystal shutter 120 to become transparent after the pixels have been reset, and ends before the application of the storage signal 113 to return to the crystal shutter 120 to an opaque state.

It is preferred that the width of signal 127 be equal to or shorter than the period starting at the end of signal 112 and ending at the beginning of signal 113 so that impinging light will not affect the photodiodes 106 or sample nodes 109 (see figure 2) during the reset process or the sample process. In addition, in imager 130 in accordance with the present invention shutter signal 127 will effectively control the photodiode 106 integration period since substantially no light will be impinging on the photodiode once the crystal shutter 120 has been rendered opaque. Thus the period identified as 115 will only determine the time between the end of reset and the beginning of sampling. In addition, in a 3T APS imager, sampling signal 113 is not required since the access transistor 111 obtains the charge level directly from the sensor node 105 (see figure 2).

This method prevents significant leakage across the photodiode 106 and, consequently, reduces the sub-threshold leakage during the period when image data in the form of charge levels is stored in the APS's.

In a further embodiment in accordance with the present invention illustrated in figure 6, a CMOS imager 150 may consist of a liquid crystal shutter 140positioned over a simple imager 100 of the type illustrated in figure 1. Thus the shutter 140 with a liquid crystal layer 117 and electrodes 118, 118' may be placed over passivity layer

103 either in contact with the layer103 or spaced from it. In this case, an insulating layer of the type discussed in figure 4 would not be required. The shutter 140 would operate in the same manner as shutter 120. This embodiment would facilitate the production processes for the imager 150 since the CMOS array 100 and the shutter 140 can be manufactured separately and then assembled.

In figure 7, an imager 170 is illustrated which is similar to the imager 130 in figure 4. However, in this particular embodiment, the shutter 160 includes multiple liquid crystal layers 117a, ...117n that are sandwiched between electrodes 118a, 118b, ...118n and 118'. This multi-layered shutter 160 may be positioned between the passivity layer 103 and the APS's 101 as shown in figure 7 or utilized in a manner similar to the imager 150 illustrated in figure 6. Multi-layered crystal shutters 160 have the advantage of assuring that the photodiodes 106 and/or sample nodes 109 will not be subjected to any light except during the integration period. Also, multiple crystal layers are capable of switching faster than a single thick crystal layer.

In a further imager 190 in accordance with the present invention, the crystal shutter 180 may be positioned at an acute angle to an imager array 100 as shown in figure 8. The crystal shutter 180 is now controlled to reflect light during the integration period and to transmit light at all other times. Such an imager would have the advantage of not having light directed to the imager array 100 except when it is reflected by the crystal shutter.

Another method of reducing charge degradation at a storage node is disclosed in conjunction with figure 9. Figure 9 illustrates a 4T ASP of the type described with respect to figure 2 where incident light 104 falling on a photodiode 106 causes a discharging of a sensor node 105 between photodiode 106 and reset transistor 107. The sensor node 105 is precharged by the reset transistor 107. The charge level is stored at a sample node 109. The sample node 109 is coupled to the gate of the output pull-up transistor 110. The source of transistor 110 is coupled to an output access transistor 111. The reset, sampling and output access transistors 107, 108 and 111 are controlled by reset 112, storage 113 and pixel access 114 signals, respectively. In figure 2, access from sample node 109 to the sensor node 105 is controlled by a sampling or storage transistor 108. Node 109 can be discharged by sub-threshold

leakage through the coupled nMOS transistor 108 and the discharge current is exponentially proportional to the gate-source and drain-source voltages of transistor 108.

In order to reduce or eliminate sub-threshold leakage resulting in a reduction of the rate of discharge of sample node 109, two or more nMOS transistors 121a ... 121N may be coupled in series as shown in figure 9 instead of the standard short transistor108 described with respect to figure 2. Initially, after the storage event controlled by signal 113, the voltage levels on sensor node 105 and sample node109 will be substantially the same, however the incident radiation 104 impinging on the photodiode 106, reduces the voltage at the sensor node 105. Any differential in voltage from the sensor node 105 to the sample node 109 initially does not discharge any but the first sampling transistor 121a. As subsequent nodes 125a ... 125(N-1) between transistors 121a ...121N become discharged, the total voltage differential is, in the worst case, equally distributed amongst the transistors 121a ...121N, resulting in a significant reduction in the sub-threshold current, and therefore a reduction in the rate of charge decay at the sample node 109.

In an alternate embodiment to reduce or eliminate sub-threshold leakage, one single long transistor 126 is substituted for the standard transistor 108 referred to in figure 2 or the set of series connected transistors 121a ... 121N referred to in figure 9. In the long transistor 126 illustrated in figure 10, the exponential time constant associated with charge decay can be more explicitly stated in that it is proportional to the relative increase in length of the sampling transistor 126.

A further embodiment of the present invention is directed to maintaining the voltage level on the storage node 109 by preventing its degradation. Miller Effect is employed to increase the capacitance of the storage node 109 with respect to high frequency response. The Miller Effect is described in the Text "Microelectronic Circuits", chapter 7.4, page 515, - Sedra and Smith 3rd Edition published by Oxford, which is incorporated herein by reference. Referring to figure 11, the 4T APS is again similar to the APS described with respect to figure 2. However, coupled to the storage node 109, is the gate of a feedback transistor 122. Transistor 122 is coupled to a current source 124 at the drain. There exists, as a part of the transistor 122, a parasitic capacitance between the feedback node 123 and the storage node 109. As the

storage node 109 voltage is degraded, the feedback transistor 122 is closed, and the voltage at the feedback node 123 rises. This increase of voltage is, in some part, conferred to the storage node 109 via parasitic capacitance. This negative feedback is known in the art as an aspect of the Miller effect, and can also be represented, in simple terms, by an increase in the gate to ground capacitance of the transistor 122.

While the invention has been described according to what is presently considered to be the most practical and preferred embodiments, it must be understood that the invention is not limited to the disclosed embodiments. Those ordinarily skilled in the art will understand that various modifications and equivalent structures and functions may be made without departing from the spirit and scope of the invention as defined in the claims. Therefore, the invention as defined in the claims must be accorded the broadest possible interpretation so as to encompass all such modifications and equivalent structures and functions.

What is claimed is:

1. A CMOS imager comprising:

- an array of active pixel sensors (APS) for individually sensing and storing incident light levels at discrete points in the array; and
- means for determining the period of time that light is incident on the active pixel sensors in the array.

2. A CMOS imager as claimed in claim 1 wherein the determining means is a liquid crystal shutter.

3. A CMOS imager as claimed in claim 2 wherein the liquid crystal shutter comprises a liquid crystal layer having an electrode layer on each side of the liquid crystal layer and the liquid crystal shutter is positioned substantialy parallel to the APS array such that the incident light impinging upon the active pixel sensors passes through the liquid crystal shutter.

4. A CMOS imager as claimed in claim 3 wherein:

- the array of active pixel sensors are fabricated on a silicon substrate;
- an insulating layer is placed over the active pixel sensors; and
- the liquid crystal shutter is positioned over the insulating layer.

5. A CMOS imager as claimed in claim 2 wherein the liquid crystal shutter comprises one or more liquid crystal layers having an electrode layer on each side of each the liquid crystal layers and the liquid crystal shutter is positioned

substantially parallel to the APS array such that the incident light impinging upon the active pixel sensors passes through the liquidcrystal shutter.

6. A CMOS imager as claimed in claim 5 wherein:

- the array of active pixel sensors are fabricated on a silicon substrate;
- an insulating layer is placed over the active pixel sensors; and
- the liquid crystal shutter is positioned over the insulating layer.

7. A CMOS imager as claimed in claim 2 wherein the liquid crystal shutter is controlled by applying different frequency signals to the shutter.

8. A CMOS imager as claimed in claim 2 wherein the liquid crystal shutter is controlled by applying different voltage level signals to the shutter.

9. A CMOS imager as claimed in claim 2 wherein the liquid crystal shutter comprises a liquid crystal layer having an electrode layer on each side of the liquid crystal layer and the liquid crystal shutter is positioned at an oblique angle to the APS array to deflect incident light onto the array.

10. A CMOS imager as claimed in claim 1 wherein the active pixel sensors each comprises a photodiode sensor node for integrating the incident light during a period of time and an access transistor to read out the charge level on the photodiode sensor node.

11. A CMOS imager as claimed in claim 1 wherein the active pixel sensors each comprises a photodiode sensor node for integrating the incident light during a period of time and a charge level storage node for storing charge level from the photodiode sensor node.

12. A CMOS imager as claimed in claim 11 wherein the active pixel sensors each further comprises two or more series connected transistors connected between the sensor node and the storage node.

13. A CMOS imager as claimed in claim 11 wherein the active pixel sensors each further comprises a long transistor connected between the sensor node and the storage node.

14. A CMOS imager as claimed in claim 11 wherein the active pixel sensors each further comprises means coupled to the storage node for increasing the voltage on the node as the charge level on the storage node degrades.

15. A CMOS imager as claimed in claim 14 wherein the voltage increasing means comprises a transistor connected to a current source with its gate coupled to the storage node.

16. A CMOS imager having an array of active pixel sensors (APS) each comprising:

- a photodiode sensor node for integrating the incident light during a predetermined period of time;
- a storage node for storing charge level from the photodiode sensor node; and

- means connected between the sensor node and the storage node to transfer the charge from the sensor node to the storage node, and to isolate the storage node from the sensing node after the transfer has been made.

17. A CMOS imager having an array of active pixel sensors (APS) each comprising:

- a photodiode sensor node for integrating the incident light during a predetermined period of time;

- a storage node for storing charge level from the photodiode sensor node; and

- two or more series connected transistors connected between the sensor node and the storage node.

18. A CMOS imager as claimed in claim17 wherein the APS's are 4T or 5T APS's.

19. A CMOS imager as claimed in claim 17 wherein the active pixel sensors each further comprises means coupled to the storage node for increasing the voltage on the node as the charge level on the storage node degrades.

20. A CMOS imager as claimed in claim 19 wherein the voltage increasing means comprises a transistor connected to a current source with its gate coupled to the storage node.

21. A CMOS imager having an array of active pixel sensors (APS) each comprising:

- a photodiode sensor node for integrating the incident light during a predetermined period of time;

- a storage node for storing charge level from the photodiode sensor node; and

- a long transistor connected between the sensor node and the storage node.

22. A CMOS imager as claimed in claim 21 wherein the APS's are 4T or 5T APS's.

23. A CMOS imager as claimed in claim 21 wherein the active pixel sensors each further comprises means coupled to the storage node for increasing the voltage on the node as the charge level on the storage node degrades.

24. A CMOS imager as claimed in claim 23 wherein the voltage increasing means comprises a transistor connected to a current source with its gate coupled to the storage node.

25. A CMOS imager having an array of active pixel sensors (APS) each comprising:

- a photodiode sensor node for integrating the incident light during a predetermined period of time;

- a storage node for storing charge level from the photodiode sensor node; and

- means coupled to the storage node for increasing the voltage on the node as the charge level on the storage node degrades.

26. A CMOS imager as claimed in claim 25 wherein the voltage increasing means comprises a transistor connected to a current source with its gate coupled to the storage node.

27. A CMOS imager as claimed in claim 25 wherein the APS's are 4T or 5T APS's.

28. A method of controlling a CMOS imager having an array of active pixel sensors (APS) for individually sensing and storing incident light levels comprising:

a. resetting the APS's substantially simultaneously;

b. allowing incident light to impinge on the APS's for a predetermined integration period;

c. storing the charge level of the incident light;

d. reading out charge levels of the APS's sequentially.

29. A method of controlling a CMOS imager as claimed in claim 28 wherein step b. includes:

b1. opening a shutter to allow incident light to impinge on the APS array; and

b2. closing the shutter after the predetermined integration period to stop incident light from impinging on the APS array.

30. A method of controlling a CMOS imager as claimed in claim 28 wherein step b. includes:

b1. causing incident light to be deflected so as to impinge on the APS array; and

b2. stopping the incident light from impinging on the APS array after the predetermined integration period.

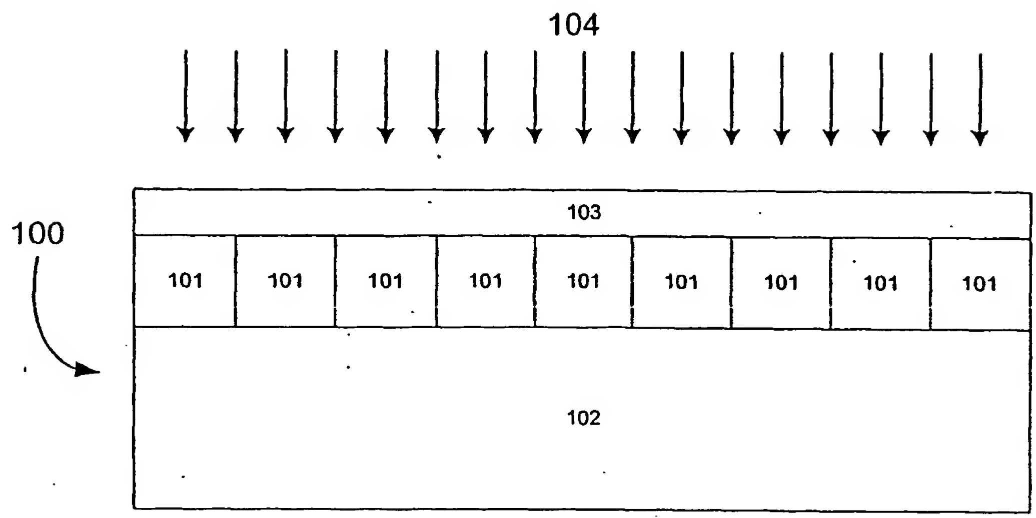


figure 1
(prior art)

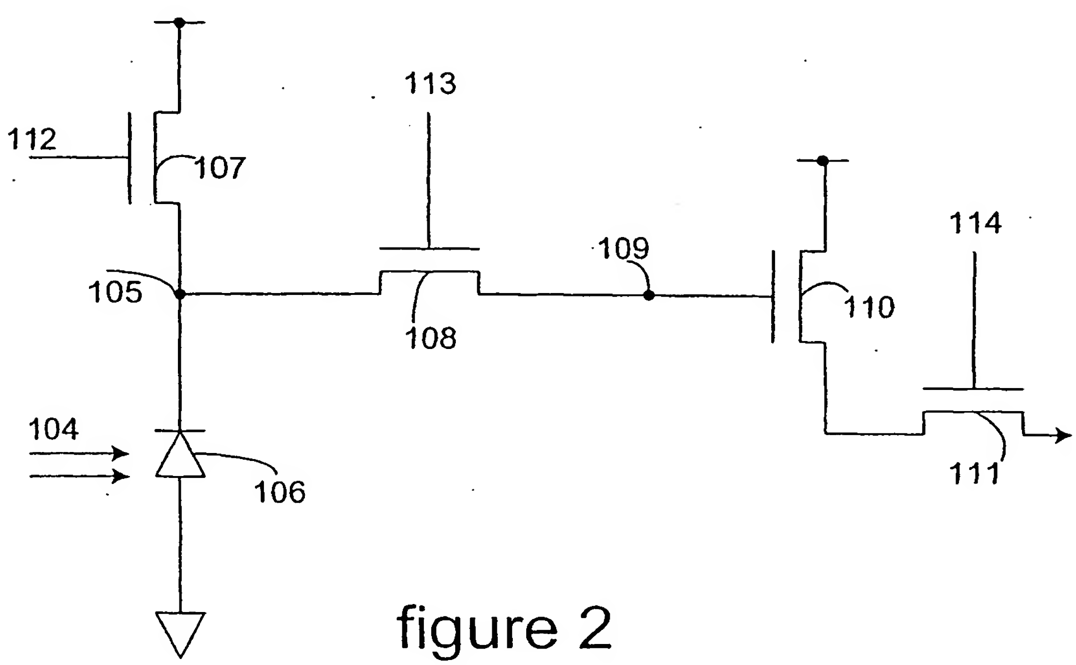


figure 2
(prior art)

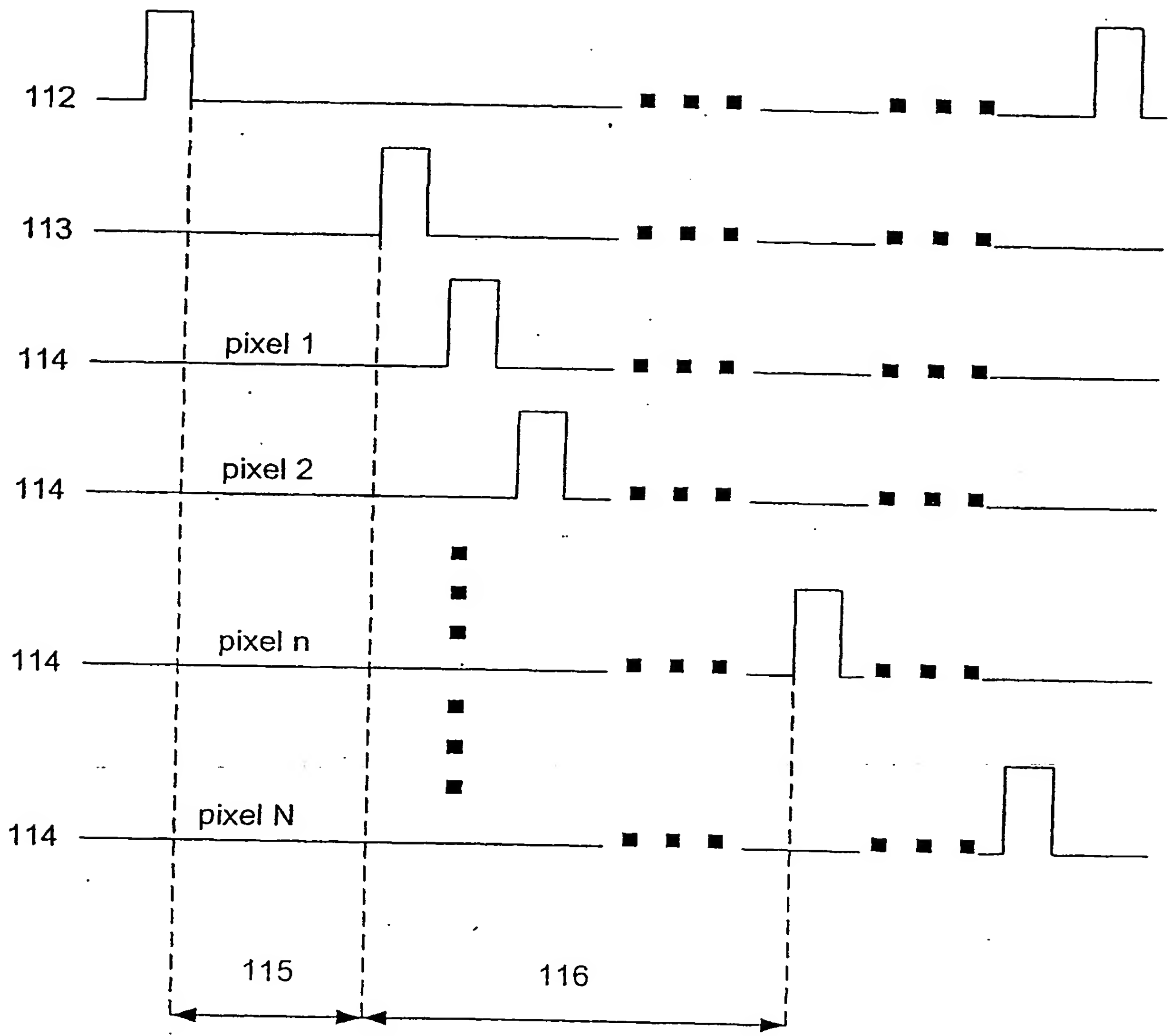
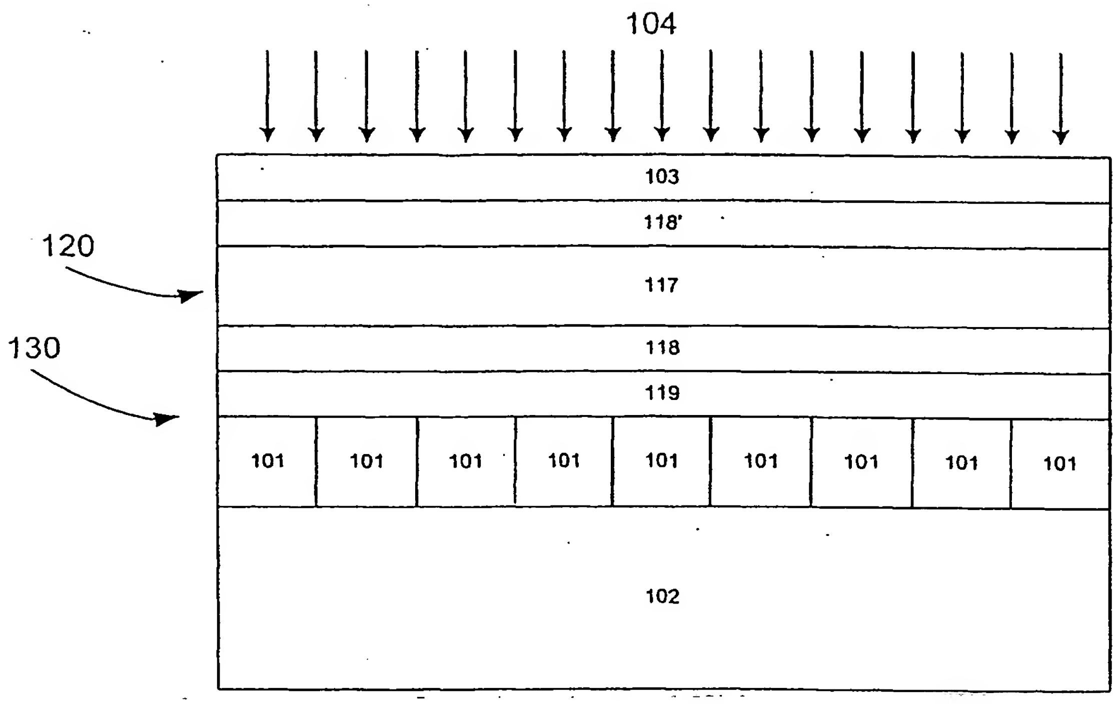


figure 3
(prior art)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118'
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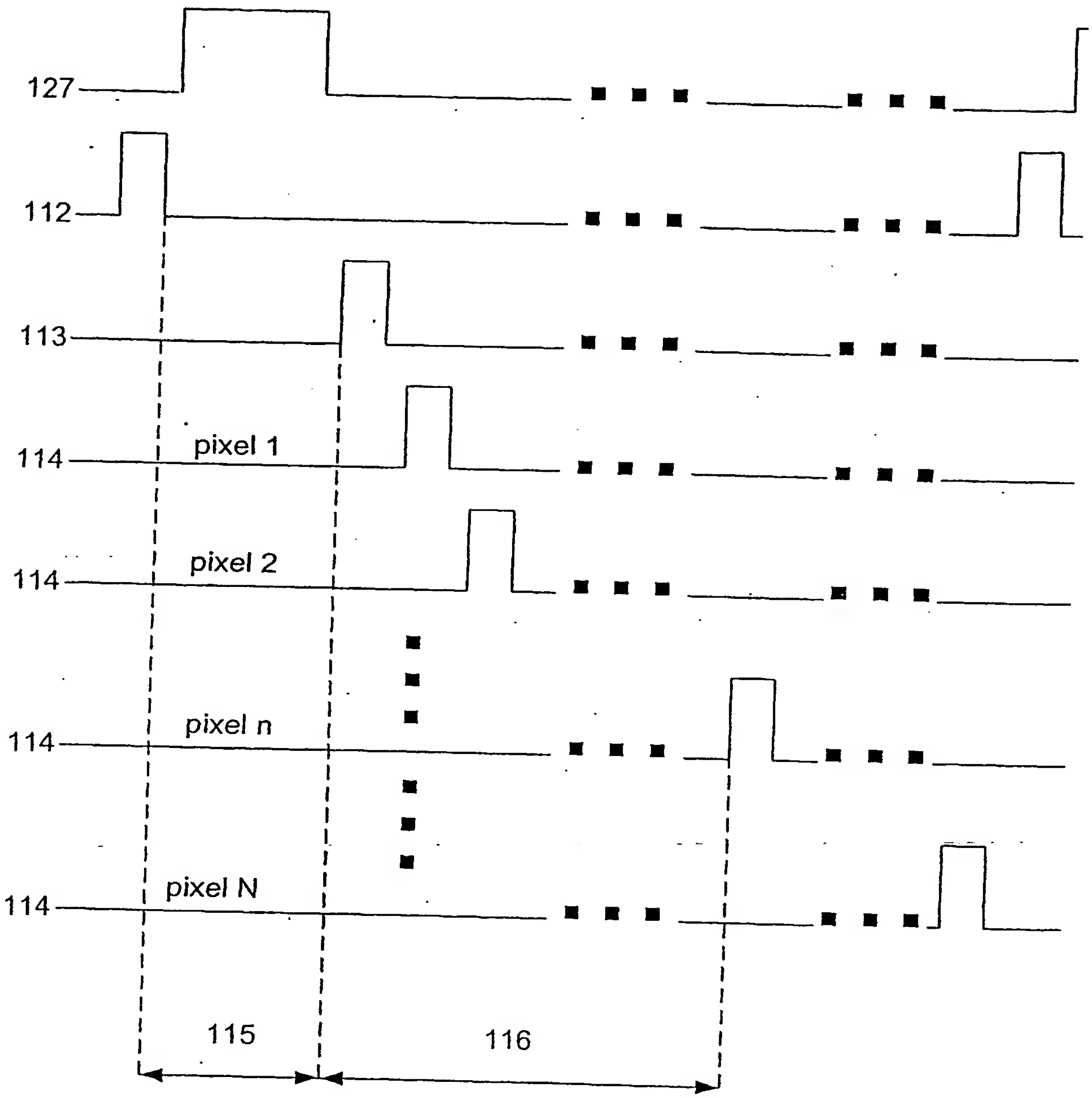
101
102
120
130

figure 4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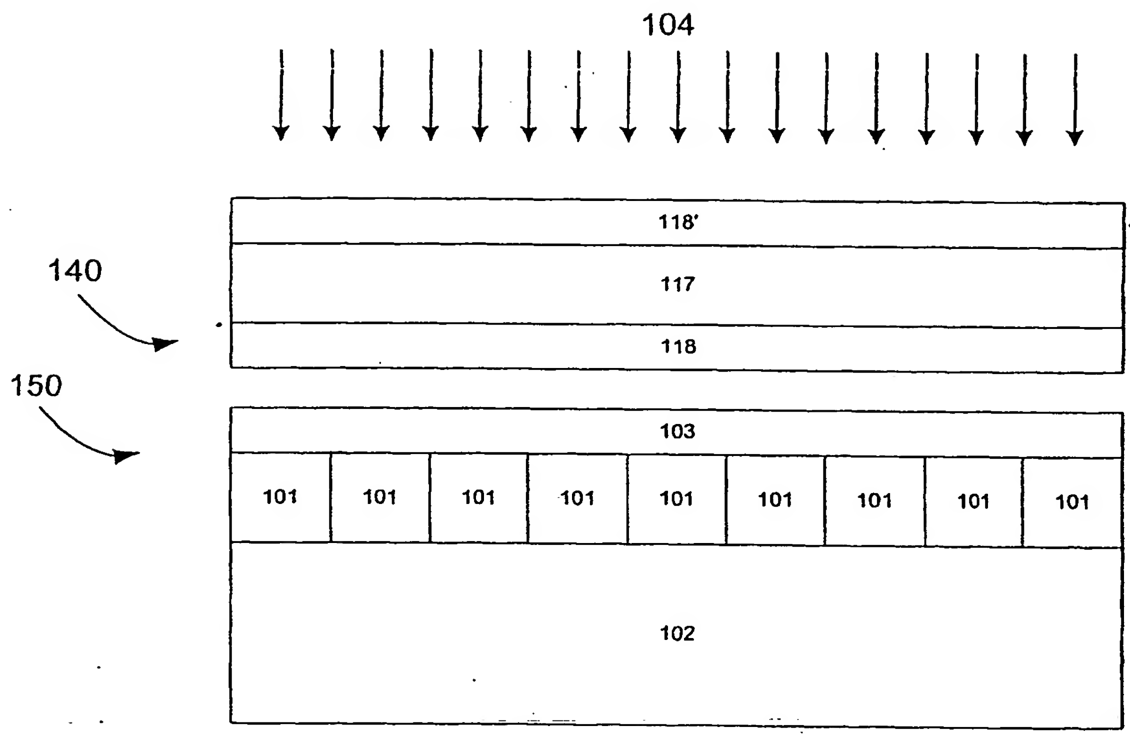
113
114
pixel 1
114
pixel 2
114
pixel n
114
pixel N
115
116

figure 5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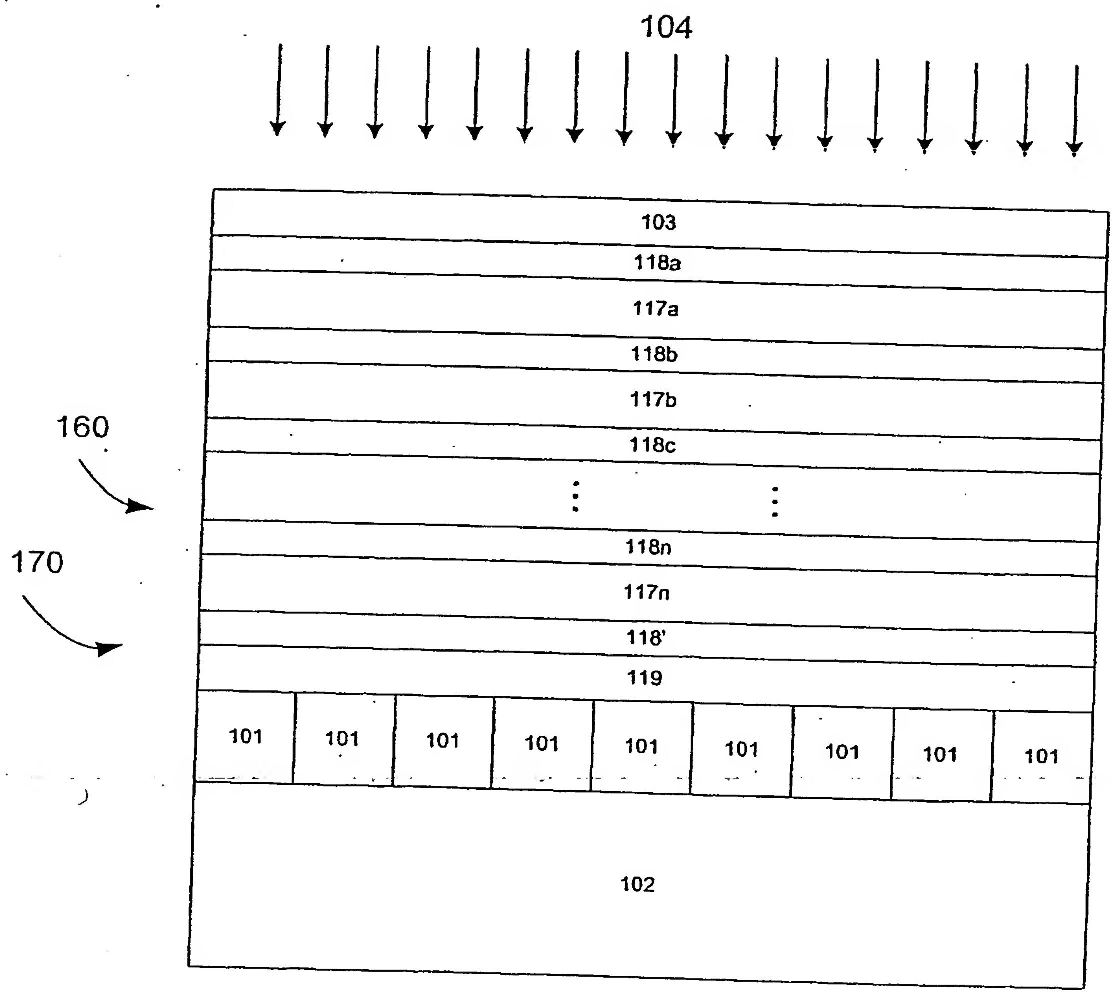
102

figure 6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101
102

figure 7

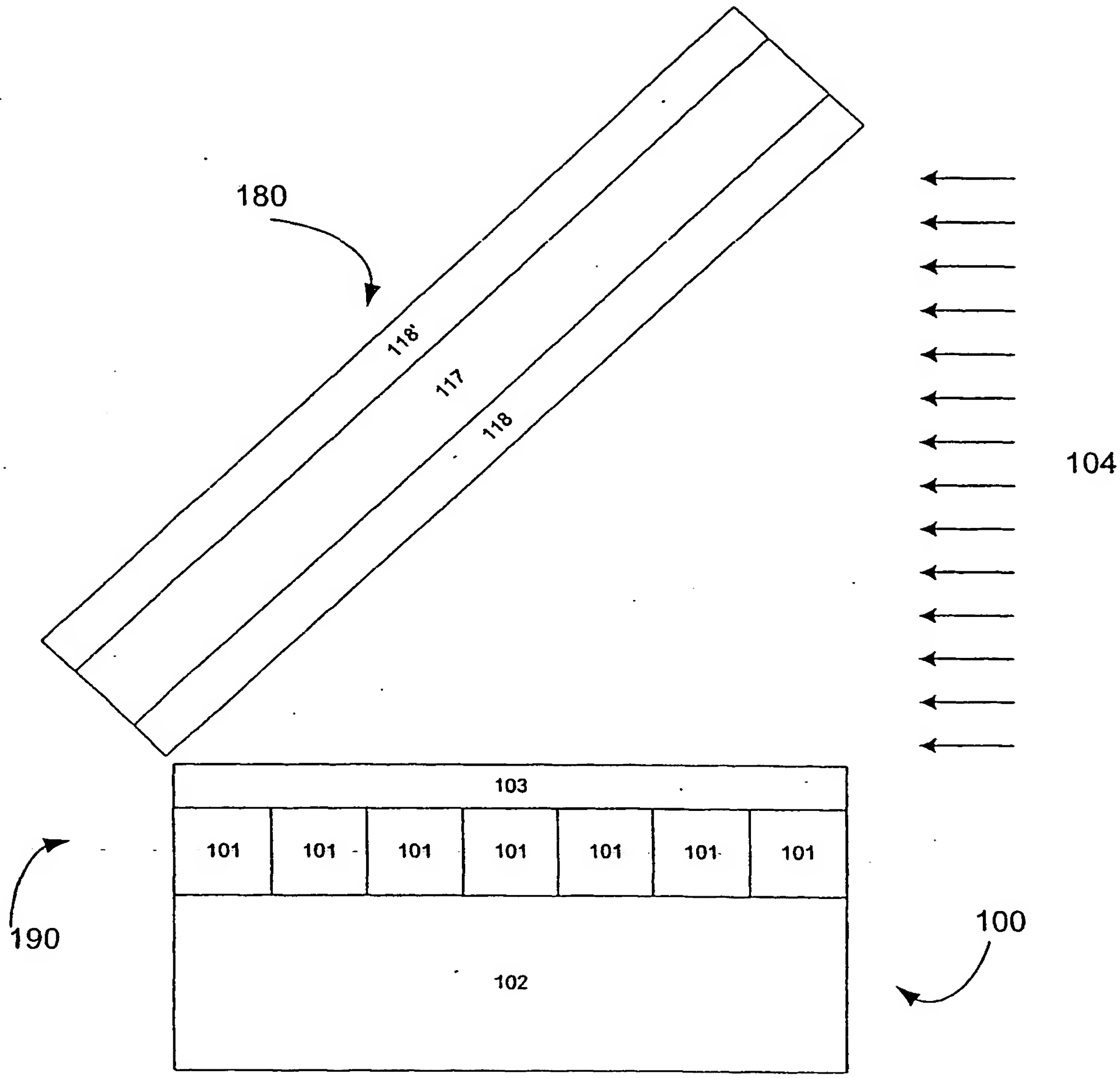

figure 8

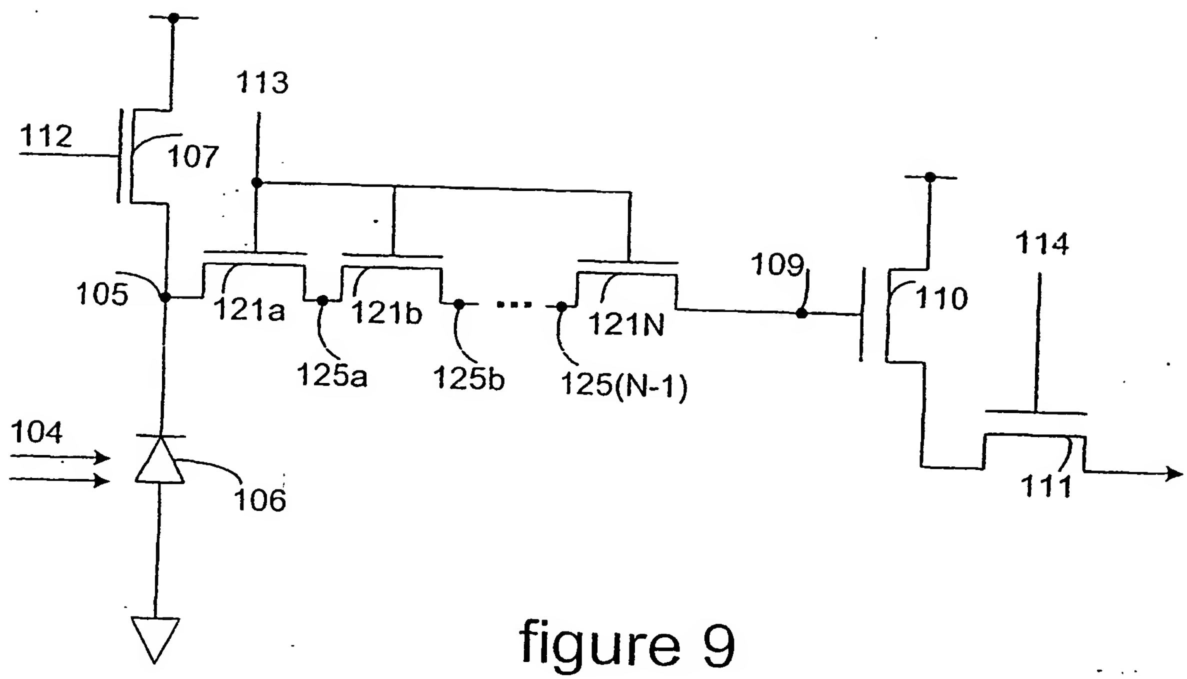

figure 9

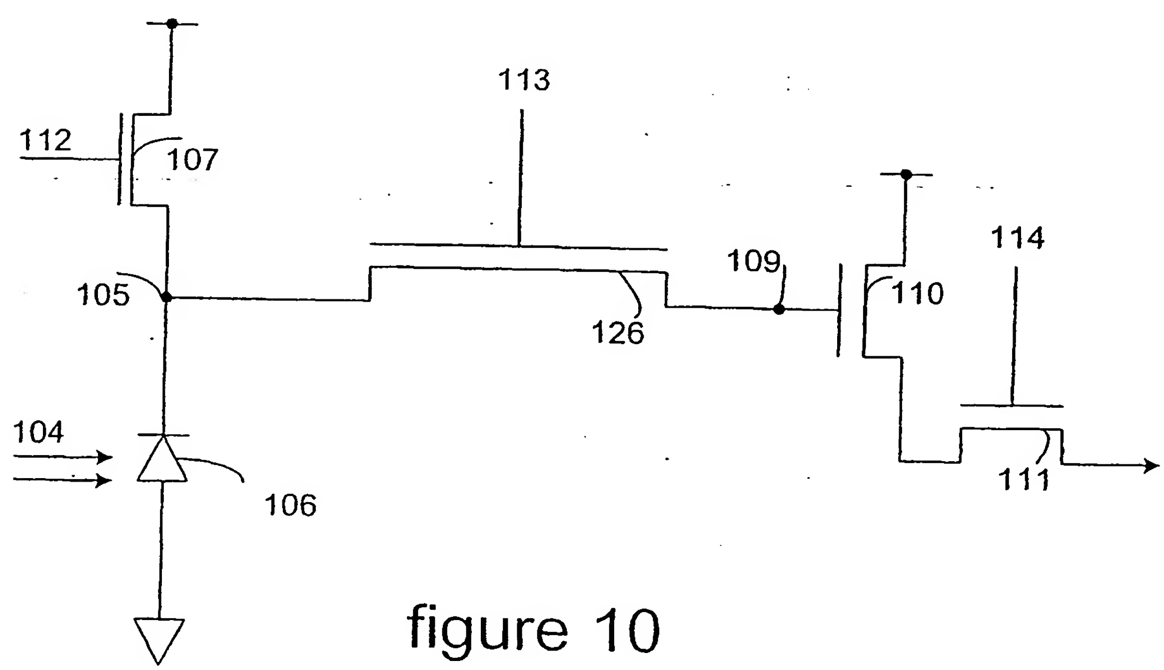

figure 10

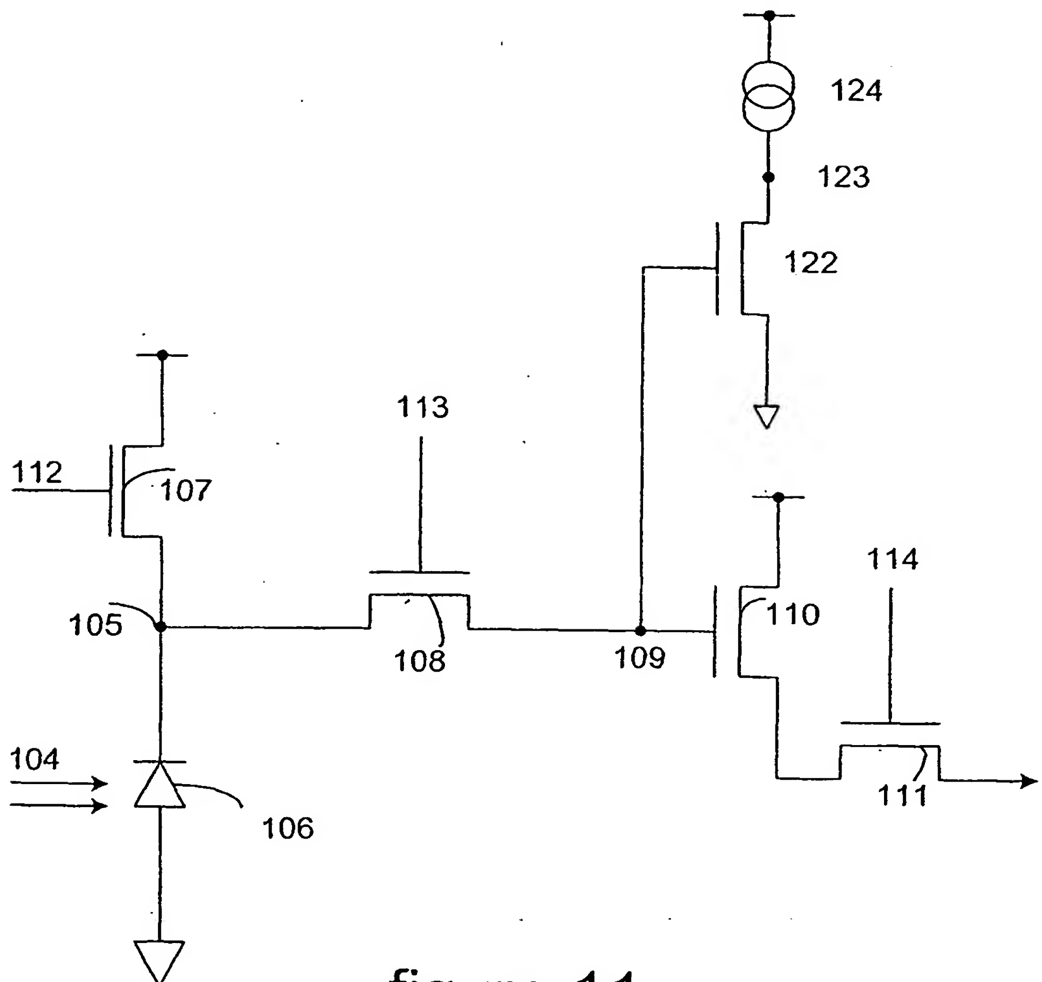

figure 11

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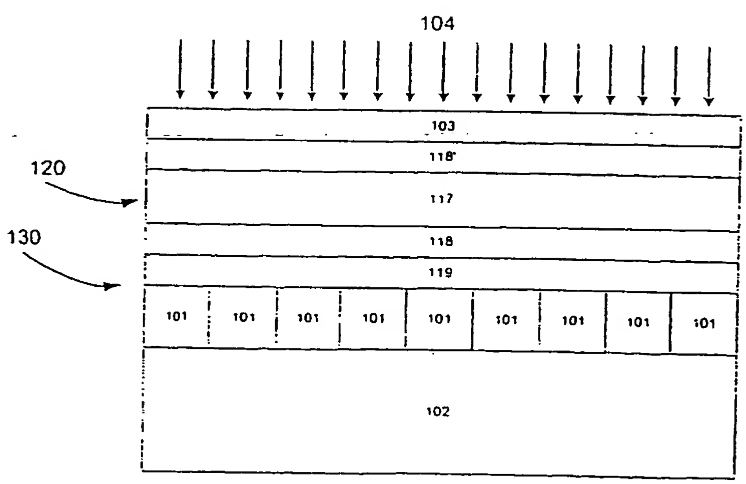
[Continued on next page]

(54) Title: CMOS IMAGER FRAME CAPTURE



(57) Abstract: A CMOS imager capable of operating in a frame capture mode. The imager has an array of active pixel sensors (APS) which sense and store incident light levels at discrete points in the array and a shutter for determining the period of time that light is incident on the array. The shutter, such as a controlled liquid crystal, may be positioned on the array surface or some distance from it, allowing incident light to pass through the shutter and impinge on the array, or the shutter may be positioned at an oblique angle to the array to reflect incident light onto the array. When the APS's in the array are 4T or 5T APS's with a sensor node and a storage node, the two nodes may be connected through two or more series connected transistors or a long transistor to prevent sub-threshold currents. Also, the storage node may be connected to the gate of a feedback transistor to raise the voltage on the storage node as the voltage on the storage node degrades.

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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	SANDINI G ET AL: "The project SVAVISCA: a space-variant color CMOS sensor" ADVANCED FOCAL PLANE ARRAYS AND ELECTRONIC CAMERAS II, ZURICH, SWITZERLAND, 18-19 MAY 1998, vol. 3410, pages 34-45, XP008001166 Proceedings of the SPIE - The International Society for Optical Engineering, 1998, SPIE-Int. Soc. Opt. Eng, USA ISSN: 0277-786X page 35, line 9 -page 38, line 27 --- -/--	1,2 4-8

[X] Further documents are listed in the continuation of box C.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
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Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Visscher, E

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
Y	PATENT ABSTRACTS OF JAPAN vol. 018, no. 144 (E-1521), 10 March 1994 (1994-03-10) -& JP 05 326903 A (SONY CORP), 10 December 1993 (1993-12-10) abstract	4-8
X	WO 99 26408 A (FOVEONICS INC) 27 May 1999 (1999-05-27) figures 3,6,8 page 8, line 22 -page 11, line 18	16,28
L,P, X	US 6 069 376 A (MERRILL RICHARD B) 30 May 2000 (2000-05-30) figures 3,6,8 column 7, line 2 -column 9, line 7	16,28
P,X	US 6 133 954 A (JIE LIANG ET AL) 17 October 2000 (2000-10-17) figures 1,2,7 column 2, line 48 -column 3, line 56 column 15, line 64 -column 16, line 20	1-3,5,7, 8,10
E	WO 01 78150 A (CSEM CT SUISSE D ELECTRONIQUE ;ISRAEL GEORG PAUL (CH); LAUXTERMANN) 18 October 2001 (2001-10-18) figure 6 page 6, line 33 - line 36	16-18
A	EP 0 511 644 A (MATSUSHITA ELECTRIC IND CO LTD) 4 November 1992 (1992-11-04) figures 1,3,4 page 3, line 6 - line 56	1-9
A	PATENT ABSTRACTS OF JAPAN vol. 1997, no. 03, 31 March 1997 (1997-03-31) -& JP 08 294059 A (CANON INC), 5 November 1996 (1996-11-05) abstract	1-9
A	PATENT ABSTRACTS OF JAPAN vol. 1995, no. 07, 31 August 1995 (1995-08-31) -& JP 07 099297 A (CANON INC), 11 April 1995 (1995-04-11) abstract	1-9
A	PATENT ABSTRACTS OF JAPAN vol. 011, no. 294 (E-544), 22 September 1987 (1987-09-22) -& JP 62 093975 A (SUMITOMO ELECTRIC IND LTD), 30 April 1987 (1987-04-30) abstract	1-9

INTERNATIONAL SEARCH REPORT

Inter Application No
PC.., ... 01/00344

Patent document cited in search report		Publication date	Patent family member(s)			Publication date
JP 05326903	A	10-12-1993	NONE			
WO 9926408	A	27-05-1999	EP	1031235	A1	30-08-2000
			TW	417390	B	01-01-2001
			WO	9926408	A1	27-05-1999
US 6069376	A	30-05-2000	NONE			
US 6133954	A	17-10-2000	NONE			
WO 0178150	A	18-10-2001	FR	2807570	A1	12-10-2001
			WO	0178150	A1	18-10-2001
EP 0511644	A	04-11-1992	DE	69221018	D1	28-08-1997
			DE	69221018	T2	22-01-1998
			EP	0511644	A2	04-11-1992
			JP	3182204	B2	03-07-2001
			JP	5122618	A	18-05-1993
			US	5532743	A	02-07-1996
JP 08294059	A	05-11-1996	NONE			
JP 07099297	A	11-04-1995	NONE			
JP 62093975	A	30-04-1987	NONE			